HIGH SPEED DATA ACCESS MEMORY ARRAYS

ABSTRACT OF THE DISCLOSURE

[0069] Techniques for reading data from memory cells in memory arrays are provided. Local read bit lines are coupled to logic gates such as NAND gates. The input terminals of each logic gate are coupled to receive signals from two of the local read bit lines. The output of the logic gate changes state when a signal on one of the local read bit lines changes state. The signal from the logic gates are transmitted to global bit lines. Memory arrays can have multiple global bit lines to reduce delays caused by resistance and capacitance on the wire. Repeater circuits can propagate a signal from one global bit line to another global bit line.